O.P.Code: 20EC0411	R20	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year II Semester Regular & Supplementary Examinations August-2023

LINEAR & DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Discuss about DC and AC characteristics of an ideal OP-AMP with relevant expressions.	CO1	L2	8M
	b	Differentiate Open-Loop & Closed Loop Op Amp Configurations.	CO1	L3	4M
		OR			
2		Draw the circuit and explain the working of the following. i) Voltage to current converter. ii) Current to voltage converter.	CO2	L3	12M

UNIT-II

3	a	Draw the circuit of a first order low pass Butterworth filter and discuss itstransfer functions.	CO1	L2	6M
	b	Explain about the operation of Wien Bridge Oscillator using Op-Amp	CO2	L3	6M
		OR			
4	a	Explain the functional block diagram of 555 timer.	CO3	L2	6M
	b	With the help of schematic diagram explain how 555 timer can be used as Monostable multivibrator.	CO3	L2	6M

UNIT-III

5	a	Draw and Explain about the Monolithic IC 565.	CO3	L2	6M
	b	Explain about R-2R Digital to Analog Converter with neat circuit.	CO4	L1	6M
		OR			
6	a	Discuss about low voltage CMOS and Interfacing.	CO4	L2	6M
	b	Explain in detail about basic ECL logic circuit.	CO4	L2	6M

UNIT-IV

7	a	Explain about functions and procedures with an example.	CO5	L2	6M
	b	Explain about libraries and packages.	CO5	L2	6M
		OR			
8		Design the logic circuit and write VHDL program for the following function.F(Y) = Π A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).	CO6	L3	12M

UNIT-V

9	a	Design a 4 to 16 decoder with 74×138 IC's.	CO6	L3	6M
	b	With the help of logic diagram explain 74×157 multiplexer.	CO6	L2	6M
		OR			
10	a	Design a synchronous 4-bit up counter.	CO6	L3	6M
	b	Write a VHDL code for the above design.	CO5	L2	6M

***** END *****